

Due: **Friday, October 12 at 9:00 pm.**

Submission: Please hand in a (tidy) paper copy at the beginning of class.

1. A Mux-Not flip-flop has two inputs, M and N . When $M = 1$, the flip-flop is toggled (i.e., its state is complemented). When $M = 0$, the next state of the flip-flop is the input value N .

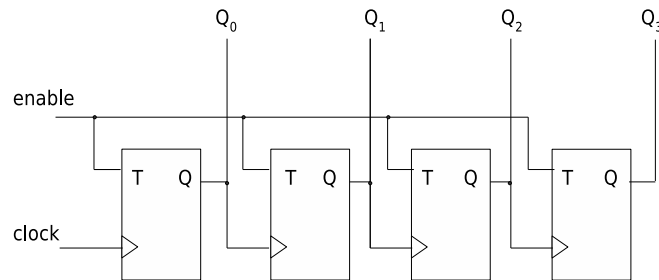
Part (a):

Give the characteristic table for a Mux-Not flip-flop.

Part (b):

Give a circuit diagram for a Mux-Not flip-flop that is based on an edge-triggered D flip-flop.

2. Consider the following circuit.



Part (a):

Give a timing diagram for this circuit, assuming the *enable* line is always held high. Your diagram should include a clock with at least 8 cycles, and timing information for each of the flip-flop outputs.

Part (b):

Give a brief description of what the circuit does.

3. Enjoy a short assignment this week!