

Due: **Friday, November 30 at 9:00 am.**

Submission: Please hand in a (tidy) paper copy at the beginning of class.

1. *Adapted from Hamacher, Vranesic, and Zaky, "Computer Organization, fifth edition"*

A word-addressable computer has a small data cache that holds 32 words, in eight 4-word blocks. Main memory holds 4K words. When a given program is executed, the processor reads data from the following sequence of hex addresses: 200, 204, 208, 20C, 2F4, 2F0, 200, 204, 218, 21C, 24C, 2F4. This pattern is repeated four times.

Suppose the cache uses direct mapping.

Hint: It may help to convert the addresses to binary, but don't convert them to decimal.

(a) Show the format of a memory address for the purpose of cache mapping, (i.e., show the number of bits needed for the tag, block, and word fields).

(b) Show the contents of the cache at the end of each pass through this loop.

A reasonable format for this might be to include a tag field and a "data" field in which you record the addresses of the words stored in a given block. For example, after reading the first word in the sequence, your cache table might look like this:

TAG	CONTENTS (represented by address)
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16	200 - 203

(c) Compute the hit rate for this example. Assume the cache is initially empty.

2. Repeat Problem 1 (all parts) for a four-way set-associative cache that uses the LRU replacement algorithm.