

CSC211
Laboratory 4

This is likely to be our last laboratory using the protoboards – so savor it!

Laboratory Exercises

1. Using TTL logic chips, build and test an S-R latch (without a clock signal). You should find that the output lines, Q and \bar{Q} , respond immediately when you change inputs S and R .
2. Now add a clock signal to your S-R latch to create a gated S-R latch. I suggest that you use one of the protoboard dip switches to simulate the clock. In other words, your circuit will have three inputs (S , R , and clock), all of which you will control manually.
You should now find that changes in S and R that happen when clock=0 are not reflected on the output lines until the clock signal rises to 1. However, when clock=1, the output lines should respond immediately to changes in S and R .
3. Modify your gated S-R latch to construct a gated D latch. (Your circuit should use the clock signal, but it will not yet be fully edge-triggered via the master-slave mechanism.) Your circuit should exhibit the characteristic table for a D flip-flop, but with the timing described in part 2.
4. *For those with extra time:* Modify your gated D latch to produce an edge-triggered (master-slave) D flip-flop. At long last, your flip-flop should change state exactly and only on the rising clock edge.