

<i>Monday</i>	<i>Laboratory</i>	<i>Wednesday</i>	<i>Friday</i>
August 27 <i>New Student Days</i>	August 28 <i>New Student Days</i>	August 29 <i>Registration</i>	August 31 Introduction to Architecture Chapter 1
September 3 Computer Organization Processors, Memory, Input/Output Chapter 2	September 4 Laboratory 1 Binary Numbers Floating-Point Numbers Data Representation on PC and Macintosh Computers Appendices A, B	September 5 Digital Logic Level Gates, Boolean Algebra Logic Circuits Sections 3.1-3.2	September 7 Digital Logic Level Memory Chips Buses Sections 3.3-3.4
September 10 Digital Logic Level Microprocessor Chips Examples Section 3.5	September 11 Laboratory 2 Designing Simple Circuits	September 12 Digital Logic Level Buses Examples Section 3.6	September 14 Digital Logic Level Examples
September 17 Digital Logic Level Interfacing Sections 3.7-3.8	September 18 Laboratory 3 Elementary Circuits and Their Uses	September 19 Digital Logic Level Circuit Design Simplifications	September 21 Microprogramming Level Microarchitecture Example: The Mic-1 Sections 4.1
September 24 Microprogramming Level Example: JVM Model Implementation Sections 4.2-4.3	September 25 Laboratory 4 Microprogramming Examples Group Exercises	September 26 Microprogramming Level Design Performance Sections 4.4-4.5	September 28 Simple C Programs Syntax and Semantics Examples <i>Take-Home Test Given Out</i>
October 1 Simple C Programs Loops Conditionals	October 2 Laboratory 5 Elementary C Programming Basic C Syntax Compiling and Running	October 3 Microcoding Summary Examples Sections 4.6-4.7	October 5 Take-Home Test Due Intro. to PC/Intel As. Lang. Instruction Format Moves/Arithmetic Section 7.1; Aulwes et al

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October 8 PC/Intel Assembly Language Run-time stack allocation Subroutines	October 9 Laboratory 6 PC/Intel Assembly Language Use of <i>pc -S</i> , <i>cc -S</i> , Interpreting Assembly Code	October 10 PC/Intel Assembly Language Comparisons, Branches	October 12 PC/Intel Machine Level Addressing Aulwes et al
October 15 PC/Intel Assembly Language Floating Point	October 16 Laboratory 7 PC/Intel Assembly Language Use of Registers Data Movements	October 17 CISC Machine Level Addressing Modes PC/Intel Instructions Section 5.4	October 19 <i>Film: The Design and Development of SPARC</i> David Patterson, UC-Berkeley
October 22 <i>Break</i>	October 23 <i>Break</i>	October 24 <i>Break</i>	October 26 <i>Break</i>
October 29 PC/Intel Assembly Language Input/Output	October 30 Laboratory 8 Additional Optimization Removing Memory References Simplification	October 31 Instr. Set Arch. Level Instruction Formats Assumptions Section 5.3	November 2 Assembly Language Level Assembly Process Macros Linking and Loading Sections 7.2-7.4
November 5 Instr. Set Arch. Level Pentium II UltraSPARC II Java Virtual Machine Sections 5.1.5-5.1.7	November 6 Laboratory 9 PC/Intel Assembly Language Project	November 7 Instr. Set Arch. Level Instruction Types VAX Instructions Section 5.5	November 9 Instr. Set Arch. Level Flow of Control RISC Instructions Comparison of RISC and CISC Section 5.6
November 12 Memory Architecture Memory Hierarchies Cache Virtual Memory	November 13 Laboratory 10 RISC Assembly	November 14 Cache Memory Principles Mapping Functions Stallings: Section 4.3	November 16 <i>Class Canceled</i>

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November 19 Cache Algorithms FIFO Least Freq. Used Least Recently Used Random	November 20 Laboratory 11 Cache Algorithms Comparison of Approaches	November 21 Memory Algorithms Paging Sections 6.1.1-6.1.5	November 23 Hour Test
November 26 Memory Algorithms Segmentation Sections 6.1.6-6.1.7	November 27 Laboratory 12 Memory Algorithms Paging Segmentation	November 28 Memory Algorithms Pentium II Memory Section 6.1.8	November 30 <i>Thanksgiving</i> <i>Recess</i>
December 3 Memory Algorithms UltraSPARC Virtual Memory, Caching Sections 6.1.9-6.1.10	December 4 Laboratory 13 I/O Approaches Examples Group Exercises	December 5 I/O Architecture Traps Interrupts Interrupt Handling Sections 5.6.4-5.6.5	December 7 Parallel Computer Arch. Design Issues Section 8.1
December 10 Parallel Computer Arch. SIMD Parallel Computers Shared-Memory Multiproc. Sections 8.2-8.3	December 11 Laboratory 14 Performance Measures Patterson/Hennessy, Chapter 2	December 12 Parallel Computer Arch. Message-Passing Multicomp. Relationship with Hardware Section 8.4	December 14 Review End-of-Course Evaluations